Design of 4-bit Flash ADC through Domino Logic in 180nm, 90nm, and 45nm Technology

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Abstract – In this paper high speed 4-bit Flash analog to digital converter (ADC) through Domino logic was proposed. The proposed Flash ADC uses appropriate combination of both domino logic based double tail comparator and domino logic based thermometer to binary code converter. Domino logic allows rail to rail logic swing. It was developed to speed up the circuit. The proposed high speed 4-bit Flash Analog to digital converter through Domino logic was designed in 180nm, 90nm, and 45nm CMOS technology in CADENCE tool with supply voltage 1.2V at sampling rate of 4GS/s. The proposed Flash ADC consumes about 738.6nw power in 180nm technology and 164.0nw power in 45nm technology with delay 650.9ps in 180nm technology and 51.33ps in 45nm technology. The physical circuit more compact than previous design compare to power and delay.

Index Terms – Comparator, Encoder, Domino logic, power, Delay.

1. INTRODUCTION

Flash analog to digital converter has the highest speed of any type of ADC. It uses one comparator per quantization level (2^N-1) and 2^N resistor string. The reference voltage is divided into 2^N values, each of which is fed into a comparator. The comparator compares the input voltage with the each reference voltage value and results the binary output in terms of '0's and '1's at the output of the comparator that is called as thermometer code which consists of string of '0's and '1's. A thermometer code exhibits all zeros for each resistor level if the value of input voltage is less than the reference voltage and one's if the input voltage is greater than or equal to the reference voltage. Block diagram of N-bit Flash ADC is shown in Fig. 1.

The praposed Flash ADC is designed using Domino logic style for reducing the power consumption and increasing the speed as compared to the current mode logic style. Related work is presented in section 2. domino logic is presented in section 3. The design of praposed comparator using dominologic is presented in section 4. The design of praposed encoder using domino logic is presented in section 5.the analysis of praposed Flash ADC and simulation results are shown in section 6 and finally conclusion in section 7.

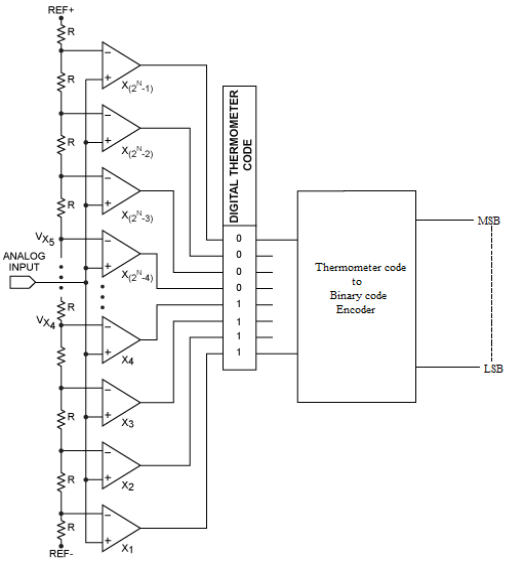

Figure 1 Block diagram of Flash ADC

2. RELATED WORK

Kriti Thakur, Sandeep Kaur Kingra [1] was praposed Design and Implementation of Hybrid 4-bit Flash ADC in 90nm CMOS technology with 1.2V supply voltage and 1GHz frequency. In this design double tail comparator is used to improve speed. For digitizing comparator yields, A multiplexer based encoder design is used. .It consume power upto 1.4mW and delay of the circuit is 1.8ns.

Liyaqat Nazir, Burhan Khurshid, et al. [2] was praposed A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique in 90nm CMOS technology. The ADC consumes 1.9807 mW from a 1.2V supply. To improve the spped TIQ based comparator is used. A simple and fast analog-to-digital converter architecture that uses pseudo-dynamic logic encoder to offer higher data conversion rates while

maintaining a low power consumption level has been proposed.the effective number of bits is 4-bits.

Parag P. Kute, Pravin Dakhole, et al. [3] was praposed Cross Coupled Digital NAND Gate Comparator Based Flash ADC in 180nm technology. This ADC is designed in TANNER S-EDIT 13. The effective number of bits is 4-bits. In this paper a digital three input NAND based comparator is constructed for the 4 bit Flash ADC. It completely eliminates the use of reference ladder, instead comparator trip points are generated by varying the width W of the transistors. Thermometer to binary decoders are presented, which shows that a multiplexer based decoder is more attractive approach since the amount of hardware and area consumption is less compared to other presented decoders and critical path is shorter. This makes design possible for low power consumption. Hence multiplexer based decoder is fast and compact for ADC implementation.

Panchal S. D., Dr. S. S. Gajre, Prof. V. P. Ghanwat [4] was proposed Design and implementation of 4-bit flash ADC using folding technique in cadence tool. In this design to improve speed folding technique is used.

Bala Dastagiri N, Abdul Rahim B,et al.[5] was praposed Domino Logic Based High Speed Dynamic Comparator in 130nm CMOS technology with 0.8V supply voltage. In this design domino logic based double tail comparator is used to improve speed. Maintaining the offset voltage stability, to improve speed, power consumption and delay, which resulted in increase in speed and a nominal change in power consumption as compared to existing double tail, and pre-amplifier based comparators. Therefore we can say that small changes in design of conventional comparator circuits there is comparativelyslight increase in speed. This design consumes power 1.7640 nw with delay 37.782ns at slew rate 10.941G.

Rahul D. Marotkar, Dr. M. S. Nagmode [6] was praposed Design of Low Power Encoder through Domino Logic for 4 Bit Flash Analog to Digital Converter in 90nm Technology using Cadence Tool with 1.2V supply voltage. The simulation results are calculated and the average power consumption of the proposed encoder is 0.01728mW which is very useful for making high speed devices as compared to the current mode logic.

Mr. K. N. Hosur, Mr. Dariyappa, Mr. Shivanand, Mr. Vijay, Mr. Nagesha, et al, [7] was praposed Design of 4 Bit Flash ADC using TMCC & NOR ROM Encoder in 90nm CMOS Technology. In this design comparator and encoder circuits are implemented using TMCC and NOR ROM encoder respectively. The output of the comparators is in the encoded form. Therefore an encoder has to be designed in order to convert the encoded signal into n bits data (digital) which is binary code. This can be done by using the ROM encoder. The power consumption of proposed ADC is 4.43mW whereas operating input frequency of 2MHz and a operating voltage of 1.8 Volt.

Marcel Siadjine Njinowa,Hung Tien Bui, et al. [8] was praposed Design of Low Power 4-Bit Flash ADC Based on Standard Cells in 180nm CMOS technology with 1.8V supply voltsge at sampling speed of 400MHz. The converter utilizes comparators created using only logic gates for converting analog input signals to digital values. To help maximize operating speed, the proposed design uses the Fat-tree method. This design consumes power 6.9mw in 180nm technology.

3. DOMINO LOGIC

There are various methods to implement the design equations for the conversion of thermometer code to binary code. Static CMOS, pseudo NMOS, dynamic logic and Domino logic are the variety of logic styles utilized for the implementation.

Static CMOS implementation is generally preferred in the noisy environment due to the property of less sensitivity towards the noise. As the circuit size increases, the number of transistor usage also increases largely which increases the power dissipation. The maximum frequency of operation of static CMOS implementation of the conversion is 1 GHz. To improve the speed, dynamic logic implementation is used. With this implementation, maximum of 4 GHz operation is attained. To further improve the speed as well as to reduce the number of transistors, pseudo NMOS logic implementation is used. By using pseudo NMOS logic, maximum of 5 GHz operation is obtained with a very high value of power dissipation. To reduce the power dissipation by keeping the frequency of operation same, Domino CMOS logic implementation is used. Smaller critical path delay, low transistor count and medium values of power dissipation and power delay product makes Domino CMOS logic implementation a preferable choice over other logic style implementation for high speed Flash ADC design. Basic diagram of Domino logic is shown in Fig. 2.

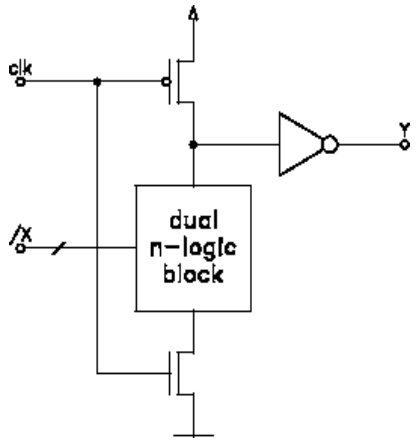

Figure 2 Basic structure of Domino logic

Domino logic consisting of the two phase when CLK=0 it occurs the "Pre-charge" phase, when CLK=1 it occurs "Evaluation" phase. In Domino logic input values is changed only during Pre-charge phase, if the value is changed during the Evaluate phase it can interrupt the output voltage.

4. COMPARATOR

Comparator can be considered as a decision making circuit because it makes a decision based on the value of input signal and reference signal. The fundamental aim of the comparator is to compare an input signal (V_{IN}) with a reference signal (V_{REF}) and to produce an output logic low or logic high depending on whether the input signal is greater or smaller than reference. The various types of comparators are generally classified into open loop comparators and regenerative comparators. Operational amplifier without frequency compensation is called open loop comparators. Regenerative comparators are mainly classified into non-clocked comparators and clocked comparators. Non-clocked comparator contains three stages namely preamplifier, decision making and output buffer. Clocked comparators are often called dynamic Comparators. The speed of clocked comparators is very high because regenerative feedback mechanism is frequently used in these types of comparators

In this paper we will take double tail dynamic comparator through domino logic as the reference model and try to optimize in terms of transistors.

This comparator is an extension of double tail comparator [5]. At the output side Domino logic circuit is added to the double tail comparator. Here the Out *n* is given to the one input and out *p* is given as another logic circuit. Considering the two stages of the circuit, at each stage the output will be taken, inverted and given as next stage input. The output of first stage and second stage considered as out1, out2 respectively. The proposed comparator is shown in Fig.3

The operation consists of two phases i.e. reset phase and comparison or regenerative phase. When CLK=0, the comparator is operated in Reset phase and CLK=V_{DD} the comparator is in comparison phase.

During reset stage i.e. CLK =0, M_{tail1} and Mtail2 are off which overcome power consumption, M_3 and M_4 pulls both output nodes F_P and F_N to V_{DD}, hence transistors M_{c1} and M_{c2} are going to cut off. The transistors between input and latch stage (M_{R1} and M_{R2}), reset inverter latch outputs to ground/V_{SS}. While the comparator at decision making/comparison stage i.e. CLK =V_{DD}, then M_{tail1} and M_{tail2} are on and transistors M_3 and M_4 are turned off. Furthermore, at the beginning of this stage, the control transistors are still off where output nodes F_N and F_P are charged to V_{DD}. Thus, the nodes F_N and F_P starts to down with different charging rates based on the applied input voltages (V_{INN} and V_{INP}). Consider the case V_{INP}>V_{INN}, the node F_N drops faster than F_P, where transistor (M_2) gives high current than the transistor (M_1). As the node F_N continues to down for a long time, the corresponding PMOS or control transistor (M_{c1}) gets to turn on, and taking F_P node gets back to the V_{DD}. So, another PMOS control transistor (M_{c2}) remains turned off, which allows the node F_N to be completely discharge.

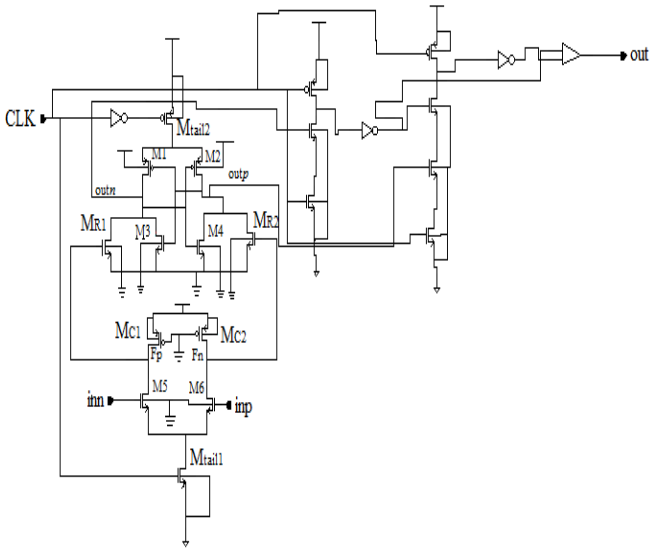

Figure 3 double tail dynamic comparator through Domino logic

5. ENCODER

We have different types of encoders for Flash ADC namely ROM encoder, fat tree encoder, multiplexer based encoder, etc. with different logic styles In this paper we will take thermometer code to binary code converter through domino logic [6] .

The comparators produce the output in a specific manner which is called thermometer code. The thermometer code is converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a vital role in the design of Flash ADC. For N-bit encoder requires 2^N inputs. Error handling capability and power dissipation are two vital parameters in the design of thermometer to binary code conversion. Offset voltage in the comparator creates bubble error in the thermometer code. These bubble errors can reduce with the help of majority of '0's and '1's. So convert the thermometer code to gray code is one of the popular methods to reduce the bubble errors in thermometer code. Block diagram of 4-bit Thermometer to binary code converter is shown in Fig. 4**.**

The equations between the thermometer code to gray code is given below and derived from the truth table 1.

$G_3 = T_8$

$G_2 = T_4\ T1_2$'

$G_1 = T_2 T_6' + T_{10} T_{14}'$

$G_0 = T_1 T_3' + T_5 T_7' + T_9 T_{11}' + T_{13} T_{15}'$

G3	G2	G1	G0	Thermometer code
0	0	0	0	000000000000000
0	0	0	1	000000000000001
0	0	1	1	000000000000011
0	0	1	0	000000000000111
0	1	1	0	000000000001111
0	1	1	1	000000000011111
0	1	0	1	000000000111111
0	1	0	0	000000001111111
1	1	0	0	000000011111111
1	1	0	1	000000111111111
1	1	1	1	000001111111111
1	1	1	0	000011111111111
1	0	1	0	000111111111111
1	0	1	1	001111111111111
1	0	0	1	011111111111111
1	0	0	0	111111111111111

Table 1 Thermometer code to Gray code Truth table

The equations between the gray code to binary is given below

$B_3 = G_3$

$B_2 = G_2 \text{ XOR } B_3$

$B_1 = G_1 \text{ XOR } B_2$

$B_0 = G_0 \text{ XOR } B_1$

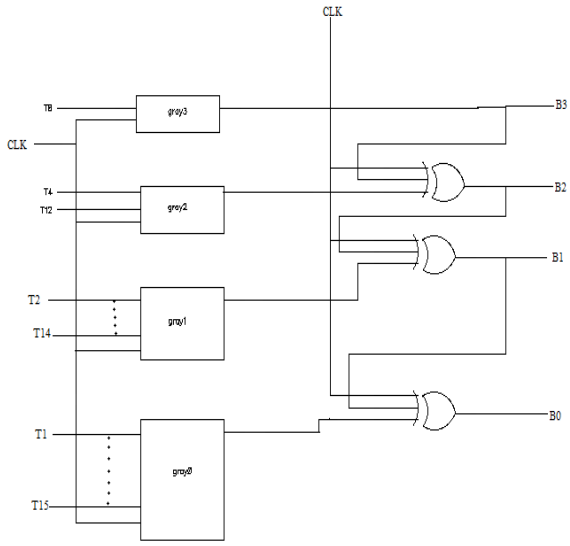

Figure 4 Block diagram of 4-bit Thermometer to binary code Converter

6. IMPLEMENTATION AND RESULTS

Flash analog to digital converter has the highest speed of any type of ADC. It uses one comparator per quantization level (2^N-1) and 2^N resistor string. The reference voltage is divided into 2^N values, each of which is fed into a comparator. Fig 7 shows the implementation of 4-bit Flash ADC.

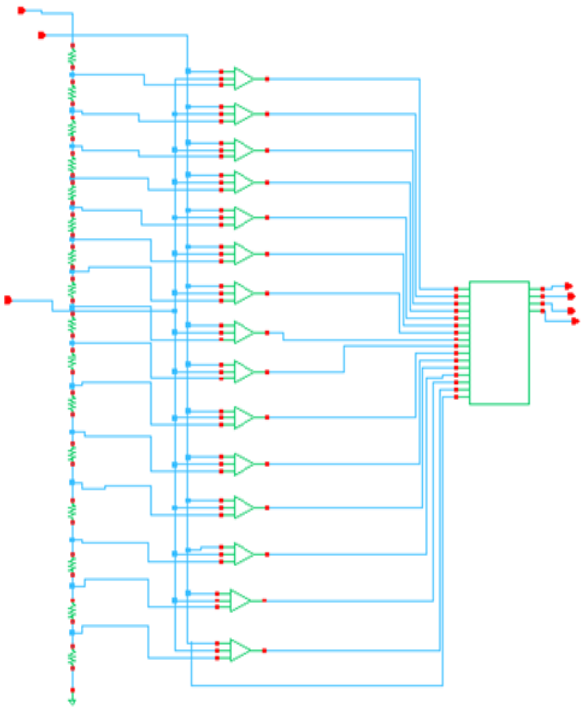

Figure 7 Schematic of 4-bit Flash ADC

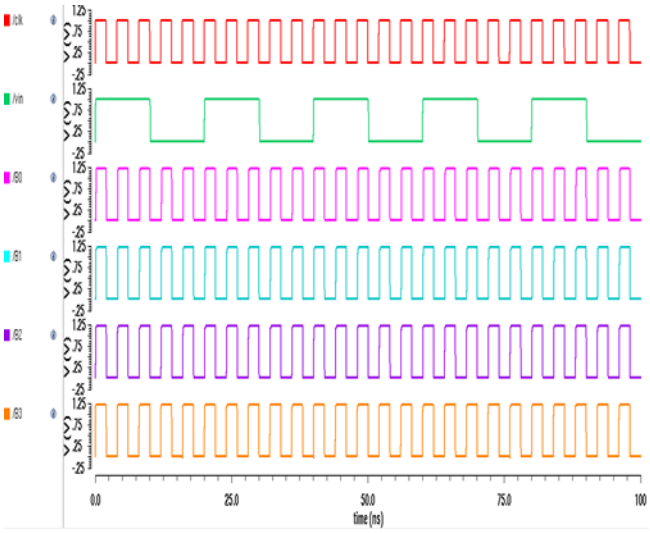

Figure 8 wave form of 4-bit Flash ADC

Technology	**180nm**	**90nm**	**45nm**
Supply voltage	1.2V	1.2V	1.2V
Power	738.6nw	171.3nw	164.0nw
Delay	650.9ps	117.1ps	51.33ps
Sampling rate	250MHZ	250MHZ	250MHZ

Table 2 Power and Delay of the Domino logic based 4-bit Flash ADC

7. CONCLUSION

Above circuits are implemented in 180 nm, 90nm, and 45nm technology using CADENCE Tool. The power dissipation for the proposed Flash ADC is reduced from in 180nm with 738.6nw to 45nm with 164nw. Also the propagation delay observed in proposed Flash ADC is 650.9ps with 180nm, which is further reduced in 45nm with 51.33ps. Offset voltage reduction can be a topic to work on in future to reduce the noise which gets In-corporate due to mismatch errors. Also further optimization can be done in order to reduce the number of transistors used in comparator design.

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